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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,971	10/26/2001	Blaine D. Gaither	10018224-1	3480

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EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,971	GAITHER ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

at page 14, line 2, application serial No. is missing.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1, 4, 5, 8, 11, 12, 14, and 16-19 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The claims recite nothing more than a nonstatutory subject matter.

Claims to computer-related inventions that are clearly nonstatutory fall into the same general categories as nonstatutory claims in other arts, namely natural phenomena such as magnetism, and abstract ideas or laws of nature which constitute "descriptive material. "Abstract ideas, Warmerdam, 33

F.3d at 1360, 31 USPQ2d at 1759, or the mere manipulation of abstract ideas, Schrader, 22 F.3d at 292-93, 30 USPQ2d at 1457-58, are not patentable. Descriptive material can be characterized as either "functional descriptive material" or "nonfunctional descriptive material." In this context, "functional descriptive material" consists of data structures and computer programs which impart functionality when employed as a computer component. (The definition of "data structure" is "a physical or logical relationship among data elements, designed to support specific data manipulation functions." The New IEEE Standard Dictionary of Electrical and Electronics Terms 308 (5th ed. 1993).) "Nonfunctional descriptive material" includes but is not limited to music, literary works and a compilation or mere arrangement of data (See MPEP section 2106, IV, B, 1).

The examiner submits that the claims are

1) not tangibly embodied on a computer readable medium; and

2) non-functional descriptive material; data *per se* is non-statutory-- this claim fails to recite the necessary functional interrelationship within the architecture to constitute a data structure.

Claims 1, 4, 5, 8, 11, and 12 recite a method that is not tied to any physical structure for processing a request. The Examiner submits that the claimed method consists solely of the manipulation of an abstract idea is not concrete or tangible. Note the steps described in claim 1, such as determining, assessing, and processing could be a mental step. The steps are not tangible. In claim 4, "an instruction message" and "operational request"; in claim 8, "memory read request" and "memory load request"; and in claim 11, "memory utilization", "memory congestion", "buffer space utilization", "bus

congestion" all are not a hardware element. The claims are non-functional descriptive material since there exist no precisely hardware elements described in the claims, therefore, directed to non-statutory subject matter.

As to claims 14, and 16-19, note a "logic" is considered as a software element. In claim 14, line 2, claim 16, line 2, and claim 17, line 1, "decode logic"; in claim 16, line 4, and claim 17, line 1, "processing logic"; in claim 18, line 1, "instruction", and claim 19, line 1, "bus controller" all are considered as a software element. Further note, in claim 14, lines 1-2, "In CPU architecture of the type that initiates both speculative and non-speculative memory requests"; and lines 4-5, "the CPU architecture processing speculative requests, or not, as a function of the conditions" are directed to an environment description only. They are not the element of the claimed invention.

In the claims, there exist no precisely hardware elements. Therefore, the claims 14, and 16-19 are software per se. which are non-functional descriptive material. The claims are not tangible and directed to non-statutory subject matter.

Claim Objections

4. Claims 2 and 3 are objected to because of the following informalities: In claim 2, line 2, "first identifier" should read -the first identifier- since it was mentioned in claim 1 previously. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 14, 15, and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 14, line 1, the phrase "of the type" renders the claim(s) indefinite because the claim(s) include(s) elements not actually disclosed (those encompassed by "of the type"), thereby rendering the scope of the claim(s) unascertainable. See MPEP § 2173.05(d).

In claim 14, line 2, "the improvement" lacks proper antecedent basis since it was not previously defined.

In claim 17, how could a logic (i.e., a software) be selected from the hardware elements such as a CPU, a chipset, a bus controller and a memory controller.

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Neufeld (U.S. Patent No. 6,567,901) (hereafter referred to as Neufeld'901).

Referring to claim 1, Neufeld'901 discloses, as claimed, a method for processing a request, comprising the steps of: determining whether the request is speculative or not based upon a first identifier (a bit encoded in the instruction, see Col. 4, lines 9-15, regarding "the instruction set of the processor 30 could be such that a compiler could predetermine the speculative or non-speculative native of the transaction 305 and pass that information to the processor 30, such as with a bit encoded in the instruction"); assessing one or both of interconnect (see Col. 6, lines 29-30, since the transactions are delivered sequentially over a single bus) and target resource conditions (see Fig. 4, since memory requests, such as 421, 422, 417, and 419 are processed, see also Col. 5, lines 47-50 for the memory requests 417 and 419 with the corresponding status of value speculative. Note for processing a speculative memory request such as 421 (see Col. 5, lines 51-53), the memory request processing logic 442 certainly will assess (or check) the target resource condition in order to complete the speculative memory request 421, see Fig. 4 and Col. 5, lines 56-60) in the event that the request is speculative; and either processing the request, or not (see Col. 5, lines 65-67, and col. 6, lines 1-2, when the memory request such as memory request 421 is cancelled), as a function of the conditions (note

processing the speculative memory request 421 (see Col. 5, lines 51-53) is based on a function of the target conditions since the memory request processing logic 442 certainly will base on the target resource condition in order to complete the memory request 421 or not, see Col. 5, lines 56-60).

Referring to claim 14, Neufeld'901 discloses, as claimed, in CPU architecture (processor 30, see Fig. 4) of the type that initiates both speculative and non-speculative memory requests (see Fig. 3, and Fig. 4, memory requests, such as 421, 422, 417, and 419 are processed), the improvement comprising decode logic for determining whether the requests are speculative (decoding a bit encoded in the instruction, see Col. 4, lines 9-15, regarding "the instruction set of the processor 30 could be such that a compiler could predetermine the speculative or non-speculative native of the transaction 305 and pass that information to the processor 30, such as with a bit encoded in the instruction"), and assessment logic for determining one or both of interconnect (see Col. 6, lines 29-30, since the transactions are delivered sequentially over a single bus) and target resource conditions (see Fig. 4, since memory requests, such as 421, 422, 417, and 419 are processed, see also Col. 5, lines 47-50 for the memory requests 417 and 419 with the corresponding status of value speculative. Note for processing

a memory request, assessing target resource condition is an inherent step), the CPU architecture (processor 30, see Fig. 4) processing speculative requests, or not (see Col. 5, lines 65-67, and col. 6, lines 1-2, when the memory request such as 421 is cancelled), as a function of the conditions (note for processing a memory request as a function of the conditions is an inherent step, see also Col. 5, lines 41-67, and col. 6, lines 1-2, for processing the memory request 421 as a function of the conditions, the memory request 421 may be cancelled based on the conditions).

Referring to claim 16, Neufeld'901 discloses, as claimed, a system for processing speculative requests, comprising: one or more requests having a bit field (a bit encoded in the instruction, see Col. 4, lines 9-15, regarding "the instruction set of the processor 30 could be such that a compiler could predetermine the speculative or non-speculative native of the transaction 305 and pass that information to the processor 30, such as with a bit encoded in the instruction") defining the requests as speculative or non-speculative; decode logic (inherently existing inside the processor 30, se Fig. 1) for decoding the bit field to determine whether one or more requests are speculative; and processing logic (inherently existing inside the processor 30, se Fig. 1) for processing speculative requests, or not, based on at least one of interconnect (see

Col. 6, lines 29-30, since the transactions are delivered sequentially over a single bus) and target resource conditions (see Fig. 4, since memory requests, such as 421, 422, 417, and 419 are processed, see also Col. 5, lines 47-50 for the memory requests 417 and 419 with the corresponding status of value speculative. Note for processing a memory request, assessing target resource condition is an inherent step).

As to claim 2, Neufeld'901 also discloses the step of determining whether the request is speculative comprises decoding first identifier as a first bit field (as set forth, a bit encoded in the instruction, see Col. 4, lines 9-15, regarding "the instruction set of the processor 30 could be such that a compiler could predetermine the speculative or non-speculative native of the transaction 305 and pass that information to the processor 30, such as with a bit encoded in the instruction") within the request.

As to claim 3, Neufeld'901 also discloses encoding the first bit field (as set forth, a bit encoded in the instruction, see Col. 4, lines 9-15, regarding "the instruction set of the processor 30 could be such that a compiler could predetermine the speculative or non-speculative native of the transaction 305 and pass that information to the processor 30, such as with a

bit encoded in the instruction") within the request to define a speculative ID of the request.

As to claim 4, Neufeld'901 also discloses the request comprising one of an instruction, message and operational request (the memory requests, such as 421, and 422 shown in Fig. 4).

As to claim 5, Neufeld'901 also discloses the step of determining a priority (see Col. 6, lines 28-30, regarding "a multiplexing of the priority with the transactions"; and Col. 6, lines 40-43, regarding "by prioritizing memory requests over a bus based on status information") of the request based upon a second identifier (see Col. 4, lines 16-24, regarding "an additional status"), in the event that the request is speculative, and wherein the step of processing the request comprises processing the request (the memory requests, such as 421, and 422 shown in Fig. 4), or not, based upon the conditions and the priority (note for processing a memory request as a function of the conditions and the priority is an inherent step, see also Col. 5, lines 41-67, and col. 6, lines 1-2, for processing the memory request 421 as a function of the conditions, the memory request 421 may be cancelled based on the conditions).

As to claim 6, Neufeld'901 also discloses the step of determining a priority comprises decoding the second identifier (see Col. 4, lines 16-24, regarding "an additional status") as a

second bit field within the request (the memory requests, such as 421, and 422 shown in Fig. 4).

As to claim 7, Neufeld'901 also discloses comprising encoding the second bit field (see Col. 4, lines 16-24, regarding "an additional status", the second bit field is inherently in the additional status) within the request to define a priority of the request.

As to claims 8, and 18, Neufeld'901 also discloses the request comprises one of a memory read request and a memory load request (the memory requests, such as 421, and 422 shown in Fig. 4).

As to claims 9, and 17, Neufeld'901 also discloses the step of determining comprises utilizing one of a CPU (the processor 30, see Fig. 4), chipset and memory controller (the memory controller 14, see Fig. 2) to determine whether the request (the memory requests, such as 421, and 422 shown in Fig. 4) is speculative.

As to claim 10, Neufeld'901 also discloses at least one of the CPU (the processor 30, see Fig. 4), chipset and memory controller (the memory controller 14, see Fig. 2) independently controls the step of processing the request (the memory requests, such as 421, and 422 shown in Fig. 4) based on the conditions.

As to claim 11, Neufeld'901 also discloses the step of assessing target resource conditions comprises assessing one or

more of memory utilization, memory congestion (since the request to be processed are the memory requests, such as 421, and 422 shown in Fig. 4), buffer space utilization (see memory request queue 401 in Fig. 4), and bus congestion (see Col. 6, lines 29-30, since the transactions are delivered sequentially over a single bus).

As to claim 12, Neufeld'901 also discloses the step of assessing interconnect conditions comprises assessing one or more of bus utilization, bus congestion (see col. 6, lines 29-30, since the transactions are delivered sequentially over a single bus), crossbar utilization, cross bar congestion, and point to point link utilization.

As to claim 13, Neufeld'901 also discloses comprising the step of notifying one or more logic devices (such as memory request processing logic 442, see Fig. 4) when the request is not processed (such as the memory request 421 is cancelled, see col. 5, lines 65-67 and Col. 6, lines 1-2).

As to claim 15, Neufeld'901 also discloses a prefetch unit (inherently existing inside the processor 30, se Fig. 1) for prefetching speculative requests (such as the speculative read in the instruction 304, see Fig. 3), wherein the decode logic detects (by detecting a bit encoded in the instruction, see Col. 4, lines 9-15, regarding "the instruction set of the processor 30 could be such that a compiler could predetermine the

speculative or non-speculative native of the transaction 305 and pass that information to the processor 30, such as with a bit encoded in the instruction") whether prefetched requests are speculative.

As to claim 19, Neufeld'901 also discloses a bus controller (inherently existing inside the processor 30, se Fig. 1) for assessing one or more of bus congestion and bus utilization conditions.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure wherein Tran et al.'9363, discloses a speculative register file for storing speculative register states and removing dependencies between instructions utilizing the register. The speculatively generated register value resulting from the modifications performed by the instructions decoded during a clock cycle is stored in a speculative register file along with constants used to generate the register value associated with each individual instruction. Abramson et al.'574 discloses a method and apparatus for performing load operations in a computer system. A load is determined ready when it is no longer blocked, such that

there is no condition which produces a resource or address dependency causing the load to be blocked.

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **TC 2100 receptionist whose telephone number is (703) 305-3900.**

11. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number:** 703-872-9306.

This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account.

Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER

June 22, 2004